

## IN THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Currently amended) ~~The apparatus according to claim 4, further comprising:~~

An apparatus for adding a plurality of partial products comprising:

a plurality of carry-save adders coupled together in series, each of the plurality of carry-save adders receiving a successive one of the plurality of partial products and two intermediate vectors (In-1, In-2) from a prior carry-save adder in the series of carry-save adders and each of the plurality of carry-save adders outputting a carry bit (Cn-1), a sum bit (Sn-1) and two intermediate vectors (In, In+1), wherein a first one in the series of carry-save adders receives two of the plurality of partial products;

a last carry-save adder coupled to a last one in the series of carry-save adders, receiving a last one of the plurality of partial products and two intermediate vectors from said last one in the series of carry-save adders, and outputting a plurality of sum bits and a plurality of carry bits;

a plurality of half-adder/full-adder series combinations coupled to the last carry-save adder, each of the plurality of half-adder/full-adder series combinations receiving two carry bits of the plurality of carry bits output by the last carry-save adder and two sum bits of the plurality of sum bits output by the last carry-save adder, and outputting two result bits and a carry bit; and

two half-adders coupled together in series and coupled to the last carry-save adder, said two half-adders receiving from the last carry-save adder two most significant carry bits and a most significant sum bit and outputting two result bits and a carry bit as a plurality of most significant bits of the result of adding the plurality of partial products.

6. (Previously presented) The apparatus according to claim 5, further comprising a single output register coupled to the plurality of half-adder/full-adder combinations and storing the two result bits and the carry bit output by each of the plurality of half-adder/full-adder series combinations.

7. (Currently amended) A method of improving the speed of a multiplier comprising the steps of:

partitioning sum and carry vectors into most significant bit and least significant bit components;

feeding the least significant bit components into a set of ripple-carry adders ~~[37-40]~~; and

using a single register in ~~the~~ an accumulation stage to accumulate the bits relating to the least significant bit components.

8. (Currently amended) The method of claim 7 wherein the set of ripple-carry adders ~~[37-40]~~ includes full-adders ~~[38-40]~~ and a half-adder 37.